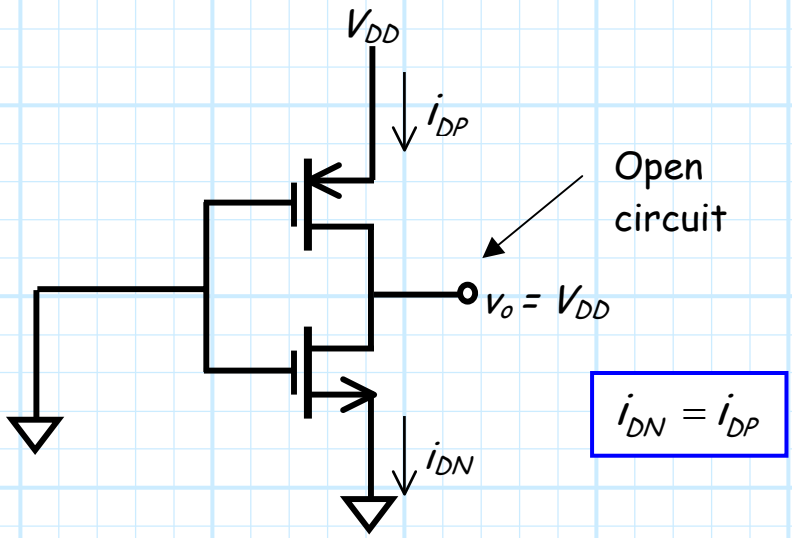
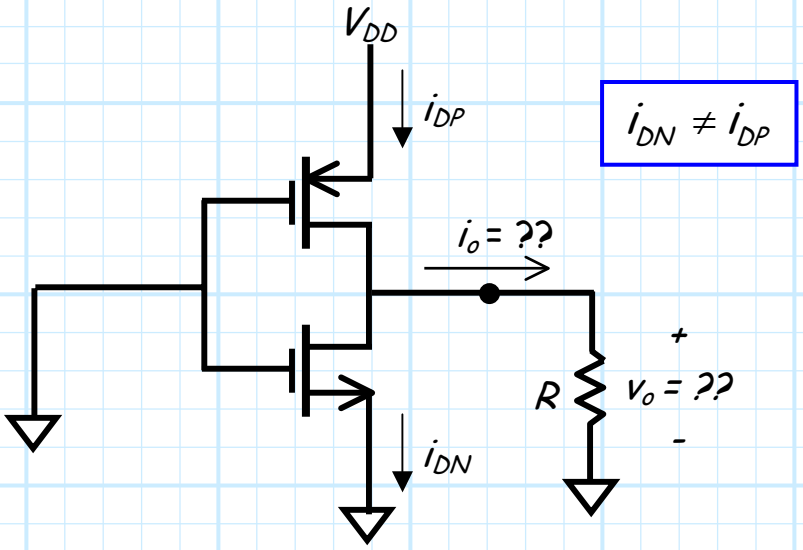
The CMOS Model

Note that **all** our analysis of a CMOS inverter has been for the case where the output is connected to an **open** circuit, for example:

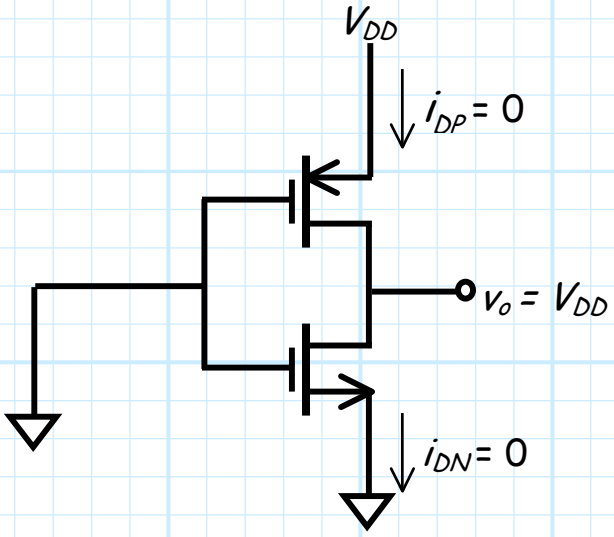


Q: *What happens if we **connect** the CMOS inverter output to **something**?*



A: Note that know we have a **very** different circuit (e.g., $i_{DP} \neq i_{DN}$). We must use **CMOS model** to analyze the circuit!

Let's **again** look at the case with an **open** circuit at the output:



In this case, Q_P is in **Triode** and Q_N is in **Cutoff**.

In other words, the channel in the NMOS device is **not** conducting, but the channel in the PMOS device **is** conducting.

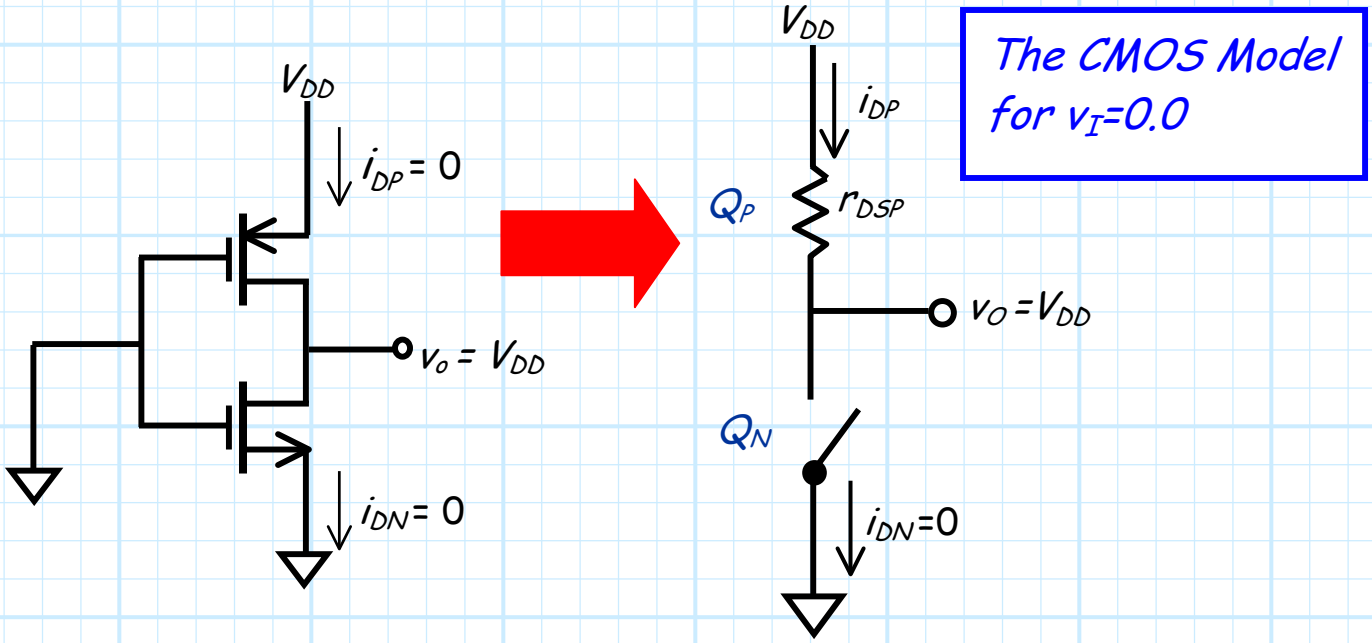
Moreover, since v_{DSP} is small (i.e., $v_{DSO} = v_O - V_{DD} = 0$ ← **really** small!!), we can use the channel resistance approximation:

$$\frac{-v_{DSP}}{i_{DP}} \approx r_{DSP} = \frac{-1}{2K\left(v_{GSP} - V_{tp}\right)}$$

In other words, the channel in the PMOS device acts like a **resistor** with resistance r_{DSP}! Since $v_{GSP} = -V_{DD}$, we find:

$$\begin{aligned} r_{DSP} &= \frac{-1}{2K\left(-V_{DD} - V_{tp}\right)} \\ &= \frac{1}{2K\left(V_{DD} + V_{tp}\right)} \\ &= \frac{1}{2K\left(V_{DD} - V_t\right)} \end{aligned}$$

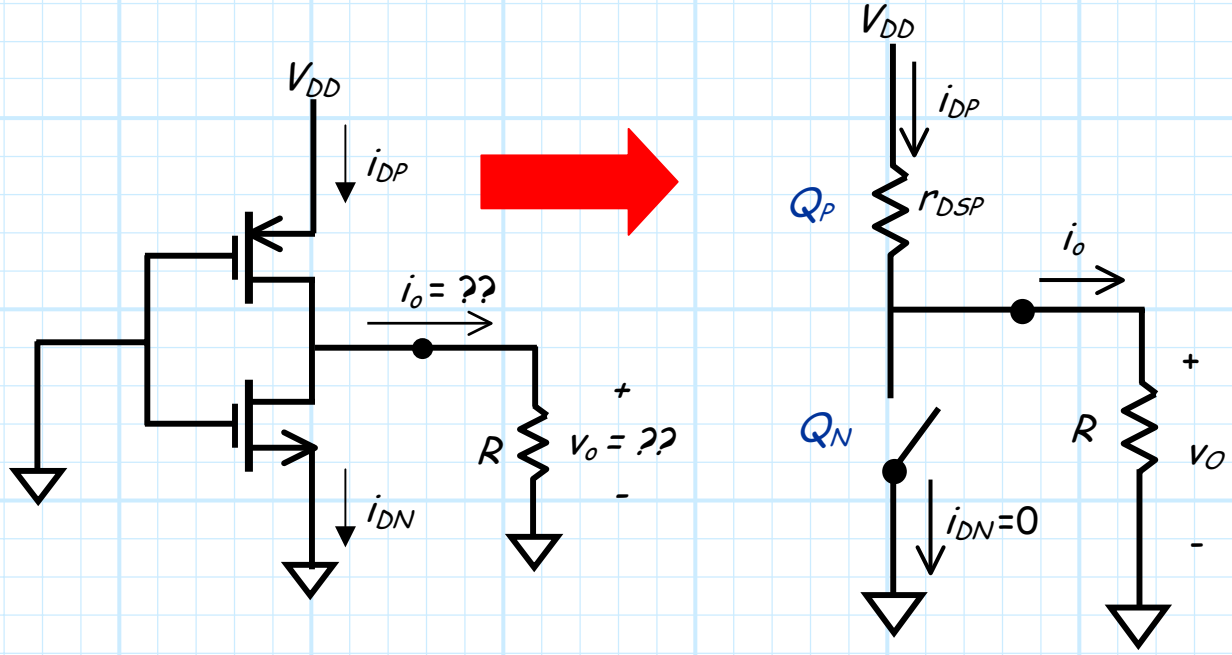
We can thus **model** the CMOS inverter as:



Note for **open** output circuit, we get the correct answer from this **model**:

$$i_D = 0 \quad \text{and} \quad v_O = V_{DD}$$

Now, let's see what happens if the output is **not open circuited**—let's place a load **resistor** at the output!:

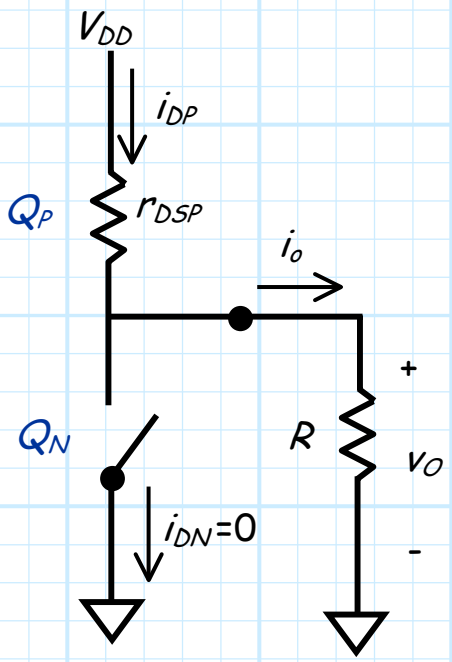


From the **model circuit**, we see that:

$$i_D = i_{DP} = \frac{V_{DD} - 0}{r_{DSP} + R} = \frac{V_{DD}}{r_{DSP} + R}$$

$$i_{DN} = 0$$

$$v_O = i_O R = V_{DD}\left(\frac{R}{r_{DSP} + R}\right)$$



Note, if $R >> r_{DSP}$, then v_O will be **slightly** less than V_{DD}!

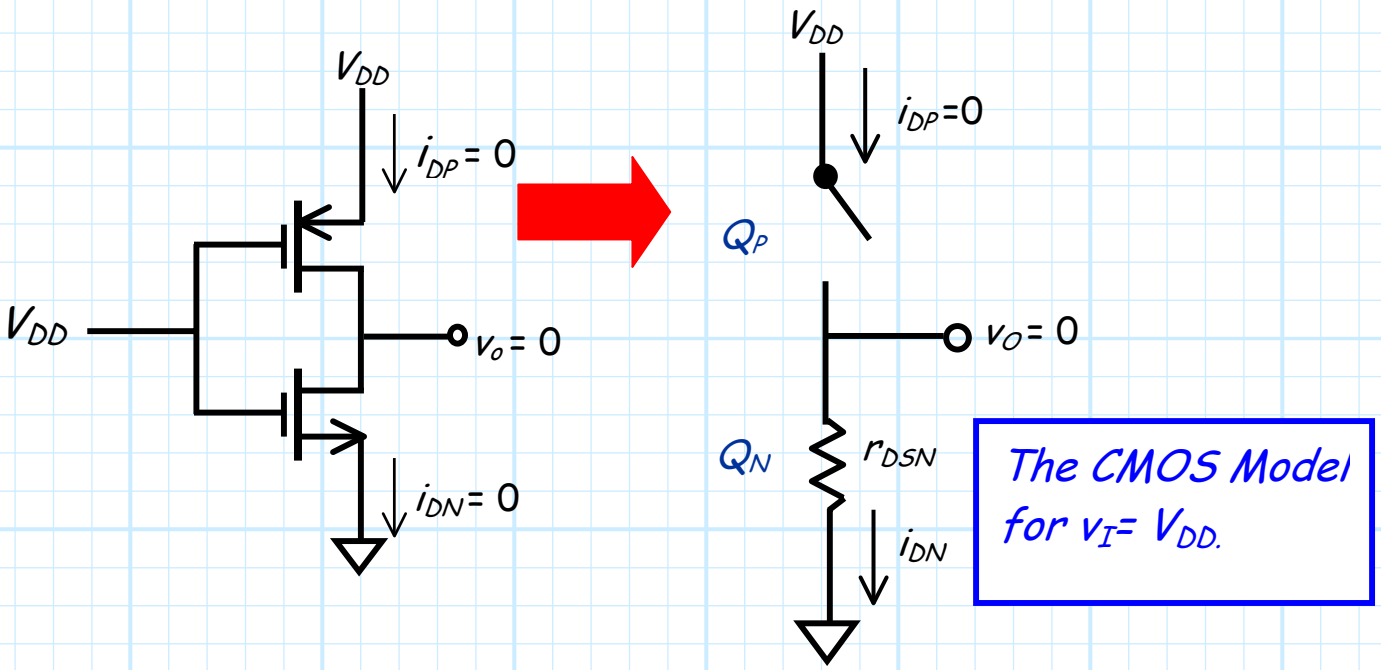
Note these are **approximate** values of i_{DP} and v_O, but if we solved the CMOS circuit directly (with **no** approximations), we would get answers **very** close to these.

In other words, the **CMOS model** is an accurate approximation provided that v_{DSP} is **small** enough.

Q: *What happens if the input voltage to the CMOS inverter is high (i.e., $v_I = V_{DD}$) ??*

In that case, **PMOS** device is in **cutoff** and the **NMOS** device is in **triode**.

Therefore the **CMOS model** for this condition is:



The CMOS Model for $v_I = V_{DD}$.

$$r_{DSN} = \frac{1}{2K\left(v_{GSN} - V_{tn}\right)} = \frac{1}{2K\left(V_{DD} - V_t\right)}$$

Note that $r_{DSN} = r_{DSP}$ in for the **two** CMOS models!